	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	84	(load same balanc$3) and time and dispatch and packet and cell	USPAT	2004/07/07 09:53			0
2	BRS	L2	79	1 and (memory or buffer)	USPAT	2004/07/07 09:54			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	362	(load same balancing) and packets and ports and (engines or processors) and (queues or memory or buffers or Fifos)	USPAT	2004/07/05 09:32			0
2	BRS	L2	125	1 and (Round same robin)	USPAT	2004/07/05 09:32			0
3	BRS	L3	46	2 and cell and (scheduler or dispatch$3)	USPAT	2004/07/05 09:34			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	560	(processors or engines) and packets and (load same balanc$3) and (input or egress) and (output or egress)	USPAT	2004/07/04 08:59			0
2	BRS	L2	513	1 and rout$3	USPAT	2004/07/04 09:00			0
3	BRS	L3	394	2 and (memory or buffer or ram or fifo) and bandwidth	USPAT	2004/07/04 09:02			0
4	BRS	L4	185	3 and stream and flow and controller	USPAT	2004/07/04 09:03			0
5	BRS	L5	146	4 and count$3 and assign$4	USPAT	2004/07/04 09:04			0
6	BRS	L6	131	5 and byte	USPAT	2004/07/04 09:04			0
7	BRS	L7	83	6 and link and cell	USPAT	2004/07/04 09:04			0
8	BRS	L8	77	7 and schedul$3	USPAT	2004/07/04 09:06			0